L Number	Hits	Search Text	DB	Time stamp
1	3	channels same ports same dma same programmable	US-PGPUB	2003/05/19 08:08
2	20	channels same dma same programmable	US-PGPUB	2003/05/19 08:08
3	257	channels same dma same programmable	USPAT; EPO; JPO; DERWENT; IBM_TDB	2003/05/19 08:21
9	14	channels same ports same dma same programmable	USPAT; EPO; JPO; DERWENT; IBM_TDB	2003/05/19 08:08
15	25	3.ti,clm,ab.	USPAT; EPO; JPO; DERWENT; IBM_TDB	2003/05/19 10:14
21	316	(priority with interrupt$3) same dma	USPAT; EPO; JPO; DERWENT; IBM_TDB	2003/05/19 10:15
27	107	(priority with interrupt$3 with transfer$4) same ((priority with interrupt$3) same dma)	USPAT; EPO; JPO; DERWENT; IBM_TDB	2003/05/19 10:17
33	30	27.ti,ab,clm.	USPAT; EPO; JPO; DERWENT; IBM_TDB	2003/05/19 10:16
39	24	(higher with priority with interrupt$3 with transfer$4) same ((priority with interrupt$3) same dma)	USPAT; EPO; JPO; DERWENT; IBM_TDB	2003/05/19 10:17

09/591,682

US-PAT-NO: 5826106

DOCUMENT-IDENTIFIER: US 5826106 A

TITLE: High performance multifunction direct memory access (DMA) controller

DATE-ISSUED: October 20, 1998

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Pang; Jianhua	Arlington	TX	N/A	N/A

US-CL-CURRENT: 710/25, 713/500

ABSTRACT:

A direct memory access (DMA) controller having memory to memory data transfer capability, a programmable fixed priority scheme, a programmable wait state, a buffer chaining mode data transfer capability, a cascade-master mode, separate channels for internal and external devices, and a programmable 8 or 16 bit requester bus size. The DMA controller includes a channel circuit connected to transfer data to and from a port, a CPU interface, a bus connected to the channel circuit and to the CPU interface to transfer data therebetween, a state machine which generates a clock signal that is used for transferring data from the channel circuit across the bus to the CPU interface, the state machine having a programmable wait state which delays the transfer of data for a preprogrammed number of clock cycles, and a data mode register which is used for setting the preprogrammed number of clock cycles.

13 Claims, 32 Drawing figures

Exemplary Claim Number: 1

Number of Drawing Sheets: 23

---------- KWIC ---------

Brief Summary Text - BSTX (12):

In another embodiment, a **DMA** controller includes a plurality of channel circuits connected to transfer data to and from a plurality of **ports**. A priority resolve circuit receives a plurality of data request signals corresponding to the plurality of channel circuits, which resolves priority among the plurality of **channels** when more than one data request signal is received, and which generates and sends a data acknowledge signal to a winning channel in response to priority being resolved, the priority resolve circuit having a **programmable** fixed priority scheme wherein the lowest priority can be assigned to any one of the plurality of **channels**. A command register is connected to the priority resolve circuit for designating which of the plurality of **channels** has the lowest priority.

US-PAT-NO: 5412656

DOCUMENT-IDENTIFIER: US 5412656 A

TITLE: Network hub for maintaining node bandwidth in a single-node network

DATE-ISSUED: May 2, 1995

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Brand; Robert C.	Andover	MA	N/A	N/A
Mantiply; Stanford L.	Palo Alto	CA	N/A	N/A

US-CL-CURRENT: 370/428, 370/466

ABSTRACT:

A hub network system is provided for communication between nodes. The system can be used, e.g., when one node can be configured for baseband bus topology communication, such as LocalTalk.TM. communication. The node can communicate using the entire bandwidth of the medium, such as 230 Kbps bandwidth, even though other nodes are connected to the network using the hub card. Preferably, the hub card includes a multiprocessor system with a shared memory for providing high internal effective bandwidth communication, such as 15 Mbps communication. A proxy scheme is provided so that the hub topology is transparent to any node which can operate as though it were configured in a bus topology.

13 Claims, 10 Drawing figures

Exemplary Claim Number: 1

Number of Drawing Sheets: 6

---------- KWIC ---------

Detailed Description Text - DETX (16):

Four data **channels** 72a, 72b, 72c, 72d couple the MPU 70 to two serial communication chips (SCC) 74a, 74b. The SCCs 74 are preferably produced by Zilog, Inc., and sold under the part number identification, Model 85C30. The MPU 70 also communicates with an I/O and interrupt control **programmable** array logic (PAL) 76. The SCCs 74 and PAL 76 cooperate to provide the MPU 70 with communication to and from four communication lines or **channels** 16a, 16b, 16c, 16d. The communication **ports** 16a, 16b, 16c, 16d are controlled by I/O **ports** 78a, 78b. The I/O **ports** 78a, 78b are controlled by cooperation between the SCCs 74a, 74b and the PAL 76. The PAL controls the SCC's using interrupt acknowledge lines 234a, 234b, I/O read signal lines 236a, 236b, and write signal lines 238a, 238b. The interrupt acknowledge lines 234a, 234b are used by the SCC's 74a, 74b to issue an interrupt signal to the MPU 70, e.g., when there is an incoming message, and is used by the MPU 70 (via the I/O and interrupt control PAL 76) to acknowledge the interrupt request. The I/O read and write signal lines 236a, 236b, 238a, 238b control the timing of read and write access to the SCC's 74a, 74b, as determined by read and write signals 239, 240 from the MPU 70, in coordination with the chip select lines 235, 237. Each SCC provides, with respect to each of the two controlled lines 16, a data channel 82a, 82b, 82c, 82d, which connects directly to the I/O port 78a, 78b,

and a control/status channel 84a, 84b, 84c, 84d, which communicates to an interface chip 86. Since there are only four direct memory access (**DMA**) **channels** 72a, 72b, 72c, 72d on the microprocessor 70, and there are four serial **ports** 16a, 16b, 16c, 16d to service, it is necessary to share the **channels** 72a, 72b, 72c, 72d between receive and transmit sides of the SCCs. This method of using the communication **channels** is acceptable, for a system such as LocalTalk.TM., which is a half-duplex system, because there is sufficient time between packets to switch the use between receive and transmit.

US-PAT-NO: 5063494

DOCUMENT-IDENTIFIER: US 5063494 A

TITLE: Programmable data communications controller

DATE-ISSUED: November 5, 1991

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Davidowski; Dennis J.	Warminster	PA	N/A	N/A
Saunders; Michael J.	Norristown	PA	N/A	N/A
O'Brien; Steven M.	Norristown	PA	N/A	N/A

US-CL-CURRENT: 709/246, 709/236

ABSTRACT:

The present invention provides a novel programmable data communications controller employed to accept data from a host computing system and for transmitting the data to a terminal designated by the host computer system. The data computer communications controller is further provided with protocols, parameters and poll tables stored in a dedicated memory of the data communications controller which enables the controller to receive data and address information from a main memory of a host computer and to reformat and pre-package the information in a protocol format block acceptable by a terminal coupled to the data communications controller. Different protocols, parameters and polls are provided in the data communications controller in the form of preprogrammed information which enables different terminals employing different protocols and protocol formats to be coupled directly to a data link interface bus without hardware modifications. Different protocols are loaded into the main memory of the main computer system and down loaded into the bit map memory of the data communications controller upon initialization of the system.

8 Claims, 7 Drawing figures

Exemplary Claim Number: 1

Number of Drawing Sheets: 7

---------- KWIC ---------

Brief Summary Text - BSTX (5):

Typical of such apparatus is found in U.S. Pat. No. 4,716,523 granted to IBM and directed to a modified direct memory access (**DMA**) controller having interrupt and arbitration features. This patent recognized that it would be desirable to combine the two above mentioned distinct architectural approaches into a single controller. In so doing, the system is provided with two distinct controllers. The prior art architecture employs arbitration logic connected to receive a request from a plurality of communication **channels** for data transfer operations. The arbitrator is configured by programming to assign a mode of data transfer operation for each channel as selected by the system user. Arbitration among competing contemporaneous request is provided by an arbitration means in the circuit and an appropriate **DMA** or character interrupt request is then given either to a **DMA** interrupt controller or to a character interrupt controller each of which resides separately and independently in the architecture of the system. This prior art system employs

one USART for each port and one port interface controller for every two **ports** or lines. The port interface controller is not **programmable and the DMA**/Interrupt Controller and Arbitrator (DAC) is factory programmed for one of the two aforementioned alternative modes of data transfer operation.

US-PAT-NO: 5561820

DOCUMENT-IDENTIFIER: US 5561820 A

TITLE: Bridge for interfacing buses in computer system with a direct memory access controller having dynamically configurable direct memory access channels

DATE-ISSUED: October 1, 1996

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Bland; Patrick M.	Austin	TX	N/A	N/A
Cronin, III; Daniel R.	Lake Worth	FL	N/A	N/A
Hofmann; Richard G.	Cary	NC	N/A	N/A
Moeller; Dennis	Boca Raton	FL	N/A	N/A
Venarchick; Lance M.	Boca Raton	FL	N/A	N/A

US-CL-CURRENT: 710/27, 710/22 , 710/26 , 710/308

ABSTRACT:

A bridge interface for buses in a computer system has a direct memory access (**DMA**) controller that controls memory transfers in the computer system. The **DMA** controller has a pair of cascaded **DMA** controller chips that provide a plurality of **DMA channels**. A multiplexer circuit receives memory address signals from the **DMA** controller chips. The memory address signals are received in both a shifted form and an unshifted form at the multiplexer inputs. By selection of the shifted or the unshifted memory address at the multiplexer, either even or odd addresses are produced at the multiplexer output for each **DMA** channel, thereby selectively providing 8-bit or 16-bit memory accesses. The control of the multiplexer is **programmable for each DMA** channel, providing dynamic configuration of the DHA **channels** as either 8-bit or 16-bit **channels**.

10 Claims, 9 Drawing figures

Exemplary Claim Number: 1

Number of Drawing Sheets: 7

---------- KWIC ---------

Abstract Text - ABTX (1):

A bridge interface for buses in a computer system has a direct memory access (**DMA**) controller that controls memory transfers in the computer system. The **DMA** controller has a pair of cascaded **DMA** controller chips that provide a plurality of **DMA channels**. A multiplexer circuit receives memory address signals from the **DMA** controller chips. The memory address signals are received in both a shifted form and an unshifted form at the multiplexer inputs. By selection of the shifted or the unshifted memory address at the multiplexer, either even or odd addresses are produced at the multiplexer output for each **DMA** channel, thereby selectively providing 8-bit or 16-bit memory accesses. The control of the multiplexer is **programmable for each DMA** channel, providing dynamic configuration of the DHA **channels** as either 8-bit or 16-bit **channels**.

US-PAT-NO: 4901234

DOCUMENT-IDENTIFIER: US 4901234 A

TITLE: Computer system having programmable DMA control

DATE-ISSUED: February 13, 1990

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Heath; Chester A.	Boca Raton	FL	N/A	N/A
Lenta; Jorge E.	Boca Raton	FL	N/A	N/A

US-CL-CURRENT: 710/40, 710/22

ABSTRACT:

A computer system in which peripherals greater in number than the number of **DMA channels** provided in the system can all have **DMA** access. Some of the **DMA channels** are dedicated to certain ones of the peripherals, while others, termed "**programmable" DMA channels,** are shared by remaining ones of the peripherals. Each peripheral having **DMA** access has a channel priority value. When a peripheral wants **DMA** access, it transmits its channel priority value onto an arbitration bus. The winning channel priority value is then compared with prestored **DMA** channel assignment values. If the comparison is successful, the corresponding peripheral is given a **DMA** channel corresponding to the **DMA** Channel assignment value with which the comparison was successful.

8 Claims, 6 Drawing figures

Exemplary Claim Number: 1

Number of Drawing Sheets: 5

---------- KWIC ---------

Abstract Text - ABTX (1):

A computer system in which peripherals greater in number than the number of **DMA channels** provided in the system can all have **DMA** access. Some of the **DMA channels** are dedicated to certain ones of the peripherals, while others, termed "**programmable" DMA channels,** are shared by remaining ones of the peripherals. Each peripheral having **DMA** access has a channel priority value. When a peripheral wants **DMA** access, it transmits its channel priority value onto an arbitration bus. The winning channel priority value is then compared with prestored **DMA** channel assignment values. If the comparison is successful, the corresponding peripheral is given a **DMA** channel corresponding to the **DMA** Channel assignment value with which the comparison was successful.

Claims Text - CLTX (11):

means for storing first and second sets of **DMA** channel assignment values, said **DMA** channel assignment values being fewer in number than the number of said peripherals and being equal in number to the number of **DMA channels** provided in said computer system, said first set of said **DMA** channel assignment values being fixed and corresponding to fixed predetermined ones of said channel priority assignment values, said second set **DMA** assignment values being

programmable and allocatable among the remaining ones of said channel priority assignment values;

US-PAT-NO: 4556952

DOCUMENT-IDENTIFIER: US 4556952 A
See image for Certificate of Correction

TITLE: Refresh circuit for dynamic memory of a data processor employing a direct memory access controller

DATE-ISSUED: December 3, 1985

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Brewer; James A.	Delray Beach	FL	N/A	N/A
Eggebrecht; Lewis C.	Rochester	MN	N/A	N/A
Kummer; David A.	Boca Raton	FL	N/A	N/A
McHugh; Patricia P.	Boca Raton	FL	N/A	N/A

US-CL-CURRENT: 711/106, 365/222 , 713/502

ABSTRACT:

In a data processing system including a dynamic RAM (14) and a **programmable,** prioritized direct memory access (**DMA**) controller (16) having a plurality of **channels,** the highest priority channel (0) is dedicated to a memory refresh operation. The system clock (P CLK) from the CPU (12) is applied to a divider counter (22) which produces a refresh clock (R CLK) having a period sufficient to generate the minimum number of refresh cycles within the minimum period required to refresh the RAM (14). The refresh clock (R CLK) is used to set a "D-type" latch (24) whose output, in turn, sets the highest priority **DMA** channel (0) request line (DREQ0), thereby initiating a memory refresh cycle. The latch (24) is cleared by the **DMA** acknowledge signal (DACK0) indicating the cycle is completed.

2 Claims, 1 Drawing figures

Exemplary Claim Number: 1

Number of Drawing Sheets: 1

---------- KWIC ---------

Abstract Text - ABTX (1):

In a data processing system including a dynamic RAM (14) and a **programmable,** prioritized direct memory access (**DMA**) controller (16) having a plurality of **channels,** the highest priority channel (0) is dedicated to a memory refresh operation. The system clock (P CLK) from the CPU (12) is applied to a divider counter (22) which produces a refresh clock (R CLK) having a period sufficient to generate the minimum number of refresh cycles within the minimum period required to refresh the RAM (14). The refresh clock (R CLK) is used to set a "D-type" latch (24) whose output, in turn, sets the highest priority **DMA** channel (0) request line (DREQ0), thereby initiating a memory refresh cycle. The latch (24) is cleared by the **DMA** acknowledge signal (DACK0) indicating the cycle is completed.

US-PAT-NO: 4075691

DOCUMENT-IDENTIFIER: US 4075691 A

TITLE: Communication control unit

DATE-ISSUED: February 21, 1978

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Davis; John Stephen	Glendale	CA	N/A	N/A
Larson; Kenneth Norman	Thousand Oaks	CA	N/A	N/A
Phalen; Frank William	Canoga Park	CA	N/A	N/A

US-CL-CURRENT: 710/64

ABSTRACT:

A communication control unit useful for operably coupling a plurality of peripheral devices to a data processing system including a central processing unit (CPU) and a main system memory. The communication control unit is comprised of three major sections: (1) A direct memory access module (**DMA**) for communicating with the memory of the CPU; (2) A serial interface adaptor module (SIA) for converting parallel data to serial data for transmission to a peripheral device and serial data to parallel data on receiving from a peripheral device; and (3) A **programmable** controller module (PCM) connected between the **DMA** and SIA for providing the overall control of message reception and transmission. The PCM comprises a small special-purpose **programmable** parallel computer. A program (firmware) stored in a read-only memory of the PCM enables the PCM to handle the different communication disciplines observed by various peripheral devices operable with the communication control unit. The program may be considered as containing two levels of instructions. The first level consists of a control program containing common routines and control programs that are used by the various communication disciplines. The second level of firmware contains all communication discipline dependent instructions associated with the processing of transmit or receive characters according to the particular discipline. Just as the first level programs are used by all the communication disciplines, the application dependent programs in the second level are used by all **channels** on the PCM I/O bus that communicate according to the discipline represented by the instructions of these programs.

5 Claims, 6 Drawing figures

Exemplary Claim Number: 1

Number of Drawing Sheets: 6

---------- KWIC ---------

Abstract Text - ABTX (1):

A communication control unit useful for operably coupling a plurality of peripheral devices to a data processing system including a central processing unit (CPU) and a main system memory. The communication control unit is comprised of three major sections: (1) A direct memory access module (**DMA**) for communicating with the memory of the CPU; (2) A serial interface adaptor module (SIA) for converting parallel data to serial data for transmission to a

peripheral device and serial data to parallel data on receiving from a peripheral device; and (3) A **programmable** controller module (PCM) connected between the **DMA** and SIA for providing the overall control of message reception and transmission. The PCM comprises a small special-purpose **programmable** parallel computer. A program (firmware) stored in a read-only memory of the PCM enables the PCM to handle the different communication disciplines observed by various peripheral devices operable with the communication control unit. The program may be considered as containing two levels of instructions. The first level consists of a control program containing common routines and control programs that are used by the various communication disciplines. The second level of firmware contains all communication discipline dependent instructions associated with the processing of transmit or receive characters according to the particular discipline. Just as the first level programs are used by all the communication disciplines, the application dependent programs in the second level are used by all **channels** on the PCM I/O bus that communicate according to the discipline represented by the instructions of these programs.

PUB-NO: WO009323810A1

DOCUMENT-IDENTIFIER: WO 9323810 A1

TITLE: SCALABLE COPROCESSOR

PUBN-DATE: November 25, 1993

INVENTOR-INFORMATION:

NAME	COUNTRY
KANAGALA, SAMEER	N/A

ASSIGNEE-INFORMATION:

NAME	COUNTRY
SEIKO EPSON CORP	JP

APPL-NO: JP09300617

APPL-DATE: May 11, 1993

PRIORITY-DATA: US88129992A (May 12, 1992)

INT-CL (IPC): G06F013/12, G06F013/28 , G06F003/06

EUR-CL (EPC): G06F013/12 ; G06F013/28

ABSTRACT:

In a computing system, a scalable coprocessor (9) for enhancing communications between a set of central processing units (CPUs) (1) and a set of system resources (2). Scalable coprocessor (9) comprises a single register file (10) compartmentalized into at least two bins, each bin corresponding to a virtual coprocessor channel. Coupled to the register file (10) is a single actual coprocessor (6, 7, 8, 13, 33) for performing operations on the system resources (2). The number of virtual **channels** can be increased arbitrarily without the need to increase the number of actual channel hardware elements. A set of **programmable** state machines (11) grants operational authority to the virtual **channels** in the order desired and for the durations desired. Embodiments of the present invention include a fly-by **DMA** controller (23), an RAID coprocessor (29), and a striping coprocessor (23).

DERWENT-ACC-NO: 1988-346279

DERWENT-WEEK: 198849

TITLE: **DMA channels** computer with **programmable** dispensing - consists of multiple peripherals assembly with channel priorities NoAbstract

PATENT-ASSIGNEE: IBM CORP[IBMC]

PRIORITY-DATA: 1987US-0030785 (March 27, 1987)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
BR 8801357 A	November 1, 1988	N/A	000	N/A
CA 1290068 C	October 1, 1991	N/A	000	N/A

APPLICATION-DATA:

PUB-NO	APPL-DESCRIPTOR	APPL-NO	APPL-DATE
CA 1290068C	N/A	1988CA-0558111	February 4, 1988

INT-CL (IPC): G06F003/00, G06F013/30

ABSTRACTED-PUB-NO: BR 8801357A

BASIC-ABSTRACT:

The computer system includes several peripherals' requiring **DMA** access. The number of peripherals is greater than the number of **DMA channels** provided in the system. Some of the peripherals are allotted fixed, dedicated **DMA channels,** while others share the remaining **channels**. The shared **channels** are called "**programmable" DMA channels**. Each of the peripherals is given a channel priority assignment. An arbitration circuit stores **DMA** channel assignment values. For each peripheral with a dedicated **DMA** channel, a fixed **DMA** channel assignment value is stored, while for the remaining peripherals, which share the **programmable DMA channels, a programmable DMA** channel assignment value is stored. When a peripheral wants **DMA** access, it transmits its channel priority value onto an arbitration bus. The highest channel priority value "wins" on the arbitration bus. The winning channel priority value is compared with the fixed and **programmable DMA** channel assignment values. If the channel priority value successfully compaeras with one of the stored fixed or **programmable DMA** channel assignment values, it is granted access to the corresponding **DMA** channel. ADVANTAGE - Avoids need for extensive modifications to operating system.

(First major country equivalent to BR8801357)

CHOSEN-DRAWING: Dwg.1/6

TITLE-TERMS: DMA CHANNEL COMPUTER PROGRAM DISPENSE CONSIST MULTIPLE PERIPHERAL ASSEMBLE CHANNEL PRIORITY NOABSTRACT

DERWENT-CLASS: T01

EPI-CODES: T01-H05B;

SECONDARY-ACC-NO:
Non-CPI Secondary Accession Numbers: N1991-255188

DERWENT-ACC-NO: 1988-280681

DERWENT-WEEK: 200010

TITLE: Computer system with direct memory access controller - has each peripheral allowed DMA access provided with arbitration circuit and assigned priority level

INVENTOR: HEATH, C A; LENTA, J E

PATENT-ASSIGNEE: INT BUSINESS MACHINES CORP[IBMC] , IBM CORP[IBMC]

PRIORITY-DATA: 1987US-0030786 (March 27, 1987)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
GB 2202977 A	October 5, 1988	N/A	016	N/A
PH 29175 A	September 26, 1995	N/A	000	G06F 003/00
DE 3810231 A	October 6, 1988	N/A	009	N/A
EP 288607 A	November 2, 1988	E	000	N/A
NL 8800715 A	October 17, 1988	N/A	000	N/A
FR 2613095 A	September 30, 1988	N/A	000	N/A
BE 1000819 A	April 11, 1989	N/A	000	N/A
NL 185106 B	August 16, 1989	N/A	000	N/A
DE 3810231 C	October 26, 1989	N/A	000	N/A
CN 8800962 A	December 14, 1988	N/A	000	N/A
US 4901234 A	February 13, 1990	N/A	010	N/A
GB 2202977 B	July 24, 1991	N/A	000	N/A
IT 1216132 B	February 22, 1990	N/A	000	N/A
EP 288607 B1	September 30, 1992	E	011	G06F 013/30
DE 3782045 G	November 5, 1992	N/A	000	G06F 013/30
ES 2035027 T3	April 16, 1993	N/A	000	G06F 013/30
KR 9508227 B1	July 26, 1995	N/A	000	G06F 013/30

DESIGNATED-STATES: AT BE CH DE ES FR GB GR IT LI LU NL SE AT BE CH DE ES FR GB GR IT LI LU NL SE

CITED-DOCUMENTS: US 3925766; US 4090238 ; US 4371932 ; WO 8002608 ; 01Jnl.Ref

APPLICATION-DATA:

PUB-NO	APPL-DESCRIPTOR	APPL-NO	APPL-DATE
GB 2202977A	N/A	1987GB-0028927	December 10, 1987
PH 29175A	N/A	1988PH-0036500	February 15, 1988
DE 3810231A	N/A	1988DE-3810231	March 25, 1988
EP 288607A	N/A	1987EP-0118545	December 15, 1987
NL 8800715A	N/A	1988NL-0000715	March 23, 1988
BE 1000819A	N/A	1987BE-0001395	December 4,

1987			
US 4901234A	N/A	1987US-0030786	March 27,
1987			
EP 288607B1	N/A	1987EP-0118545	December 15,
1987			
DE 3782045G	N/A	1987DE-3782045	December 15,
1987			
DE 3782045G	N/A	1987EP-0118545	December 15,
1987			
DE 3782045G	Based on	EP 288607	N/A
ES 2035027T3	N/A	1987EP-0118545	December 15,
1987			
ES 2035027T3	Based on	EP 288607	N/A
KR 9508227B1	N/A	1988KR-0002038	February 27,
1988			

9508227 B1
INT-CL (IPC): G06F003/00, G06F009/06 , G06F013/30 , G06F013/36

ABSTRACTED-PUB-NO: DE 3810231C

BASIC-ABSTRACT:

A CPU communicates with a main memory (15), bus controller (16) and math co-processor (14) via a system bus (26). Communication between the CPU and its associated peripheral devices is through the bus controller, which is coupled to the peripheral devices through a family bus (25). The peripheral devices may include an auxiliary memory (17), two communications devices (18 and 19), a hard file (20), an optical disc (21) and two floppy discs (23). Other peripherals can be used as system needs dictate. The peripheral devices are represented generically by DMA slave (24).

A DMA controller (12) is provided to allow at least selected ones of the peripheral devices direct memory access. For this purpose the family bus is branched to the DMA controller. Each peripheral allowed DMA access is provided with an arbitration circuit (24) and each peripheral having an arbitration circuit is assigned an arbitration (priority) level. A central arbitration control circuit (11) is associated with the DMA controller to arbitrate among peripheral devices concurrently requesting DMA access and to inform the DMA controller of which peripheral is to have access.

ADVANTAGE - Increased data transfer rates, improved system efficiency.

ABSTRACTED-PUB-NO: EP 288607B

EQUIVALENT-ABSTRACTS:

A CPU (10) communicates with peripheral devices (17-24) over a centralbus system (16,25,26). Direct memory access (DMA) requests to the CPU are handled by control and arbitration units (11,12) over several DMA channels some of which are allocated one peripheral (17-24) and the remainder a number of peripherals (17-24). An arbitration circuit (28) in a peripheral (24) selects a peripheral according to an arbitration level value and this value is programme set in a register (70) in the peripheral (24). The corresponding value is also programme stored in register and hardwired switches in the main arbitration unit (11) where it is compared with the value on the bus (25) from the peripheral (24) to initiate a DMA handshake if the comparison is true. The multi-peripheral DMA channels are pre-programmed and the single-peripheral channels are hard wired in the comparison logic circuits in the central arbitration unit (11). USE/ADVANTAGE - Ensures that no peripheral is desired direct memory access.

(9pp)

A computer system comprising a multi-channel direct memory access (DMA) device (12), and common bus means for coupling a plurality of peripheral devices (17-24) to the DMA device, said common bus means being capable of coupling a number of peripheral devices, greater than the number of DMA channels, to the DMA device, at least one DMA channel being shared between peripheral devices through an arbitration control circuit (11), the system being characterised in that each peripheral device seeking access to said common bus applies a respective channel assignment value associated therewith to the bus, a device obtaining access to the bus leaving its channel assignment value on the bus, the arbiration control circuit (11) comprising means in each channel of the DMA device for comparing (42, 43) the channel assignment value from a peripheral device requesting access to a DMA channel with channel assignment data programmed into the arbitration control circuit to determine current access to its respective channel.

GB 2202977A

GB 2202977B

A computer system comprising a multi-channel direct memory access (DMA) device (12), and means for coupling a plurality of peripheral devices (17-24) to the DMA device, said means for coupling being capable of coupling a number of peripheral devices, greater than the number of DMA channels, to the DMA device, the system being characterised in that each peripheral device has a respective channel assignment value associated therewith and at least one DMA channel is shared between periph eral devices through an arbitration control circuit (11), the arbitration control circuit (11) comprising means for comparing (42,43) the channel assignment value from a perip

US 4901234A

Peripherals greater in number than the number of **DMA channels** provided in the system can all have **DMA** access. Some of the **DMA channels** are dedicated to certain ones of the peripherals, while others, termed "**programmable" DMA channels,** are shared by remaining ones of the peripherals. Each peripheral having **DMA** access has a channel priority value. When a peripheral wants **DMA** access, it transmits its channel priority value onto an arbitration bus. The winning channel priority value is then compared with prestored **DMA** channel assignment values. If the comparison is successful, the corresponding peripheral is given a **DMA** channel corresponding to the **DMA** Channel assignment value with which the comparisons was successful. USE/ADVANTAGE - Micro or minicomputer system. Each peripheral device allowed **DMA** access is assigned its own **DMA** access arbitration level.

(10pp)

CHOSEN-DRAWING: Dwg.1/6

TITLE-TERMS: COMPUTER SYSTEM DIRECT MEMORY ACCESS CONTROL PERIPHERAL ALLOW DMA ACCESS ARBITER CIRCUIT ASSIGN PRIORITY LEVEL

DERWENT-CLASS: T01

EPI-CODES: T01-H05B;

SECONDARY-ACC-NO:
Non-CPI Secondary Accession Numbers: N1988-213080

DERWENT-ACC-NO: 1988-237250

DERWENT-WEEK: 198834

TITLE: Direct memory access system for single IC micro-controller - has three 16-bit registers as source address register and one 8-bit register as control register for each of two DMA channels

INVENTOR: BORKAR, S; PAWLOSKI, M ; WHITE, J

PATENT-ASSIGNEE: INTEL CORP[ITLC]

PRIORITY-DATA: 1987US-0015799 (February 17, 1987)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
GB 2201269 A	August 24, 1988	N/A	030	N/A
GB 2201269 B	April 17, 1991	N/A	000	N/A
US 4782439 A	November 1, 1988	N/A	013	N/A

APPLICATION-DATA:

PUB-NO	APPL-DESCRIPTOR	APPL-NO	APPL-DATE
GB 2201269A	N/A	1988GB-0000644	January 13, 1988
US 4782439A	N/A	1987US-0015799	February 17, 1987

INT-CL (IPC): G06F013/28

ABSTRACTED-PUB-NO: GB 2201269A

BASIC-ABSTRACT:

The two DMA channels which are identical to one another, allow high speed data transfer from one variable memory space to another. As many as 64 Kbytes can be transferred in a single DMA operation. The memory transfer can be between two parts of the same RAM from a RAM to an external memory, from an external memory to the RAM and between two parts of the external memory.

The **DMA channels** are software **programmable** to operate in either block mode or demand mode. In block mode, **DMA** transfers can be further programmed to take place in burst mode or alternate cycle mode. In burst mode, the processor halts its execution and dedicates its resources towards the **DMA** transfer. In alternate cycle mode, the **DMA** cyles and processor instruction cycles occur alternately.

ADVANTAGE - Provides transfer of data directly to and from RAM and peripheral device, i.e. without using processor or its registers.

ABSTRACTED-PUB-NO: GB 2201269B

EQUIVALENT-ABSTRACTS:

An integrated circuit microcontroller having a bus, an arithmetic logical circuit, a random access memory coupled to said bus, an external memory for coupling to said bus, and at least one port driver for coupling to external

devices, said random access memory and said external memory being directly accessible by said external devices through said at least one port driver, said microcontroller comprising: (a) at least two channels coupled to said bus for directly accessing at least one of said memories to selectively effect the transfer of data from (i) a first portion of said random access memory to a second portion of said random access memory; (ii) a portion of said random access memory to a portion of said external memory; (iii) a portion of said external memory to a portion of said random access memory; and (iv) a first portion of said external memory to a second portion of said external memory; (b) direct memory access control means coupled to said bus, said at least one port driver and said at least two channels for generating channel control signals for said at least two channels based upon signals on said bus, and said at least one port driver, said channel control signals for controlling the operation of said at least two channels; wherein each of said channels comprises: (i) a control register for storing the status of the channel; (ii) a source address register for storing the address of a byte in said internal memory or external memory to be transferred; (iii) a destination address register for storing the address of a byte in said internal memory or external memory; and (iv) a byte count register for storing the number of bytes remaining to be transferred by said channel.

US 4782439A

The on-board DMA channels are used in connection with a single integrated circuit microcontroller. The two DMA channels, which are identical to one another, allow high speed data transfer from noe variable memory space to another. As many as 64 Kbytes can be transferred in a single DMA operation. The memory transfer can be between internal data memory, external data memory and/or special function registers (of the type commonly employed in INTEL 8051 microcontrollers). (13pp)

CHOSEN-DRAWING: Dwg.2A/7

TITLE-TERMS: DIRECT MEMORY ACCESS SYSTEM SINGLE IC MICRO CONTROL THREE BIT REGISTER SOURCE ADDRESS REGISTER ONE BIT REGISTER CONTROL REGISTER TWO DMA CHANNEL

DERWENT-CLASS: T01

EPI-CODES: T01-H05B;

SECONDARY-ACC-NO:
Non-CPI Secondary Accession Numbers: N1988-180284

L Number	Hits	Search Text	DB	Time stamp
1	3	channels same ports same dma same programmable	US-PGPUB	2003/05/19 08:08
2	20	channels same dma same programmable	US-PGPUB	2003/05/19 08:08
3	257	channels same dma same programmable	USPAT; EPO; JPO; DERWENT; IBM_TDB	2003/05/19 08:21
9	14	channels same ports same dma same programmable	USPAT; EPO; JPO; DERWENT; IBM_TDB	2003/05/19 08:08
15	25	3.ti,clm,ab.	USPAT; EPO; JPO; DERWENT; IBM_TDB	2003/05/19 08:21

PAT-NO: JP02000207352A

DOCUMENT-IDENTIFIER: JP 2000207352 A

TITLE: MEMORY ACCESS CONTENTION CONTROL METHOD, CIRCUIT THEREFOR AND DATA PROCESSOR

PUBN-DATE: July 28, 2000

INVENTOR-INFORMATION:

NAME	COUNTRY
TAMURA, YOSHIHIRO	N/A
NAGATA, TETSUYA	N/A

ASSIGNEE-INFORMATION:

NAME	COUNTRY
HITACHI COMMUN SYST INC	N/A

APPL-NO: JP11006916

APPL-DATE: January 13, 1999

INT-CL (IPC): G06F013/28, G06F013/30 , G06F013/362

ABSTRACT:

PROBLEM TO BE SOLVED: To make the bus request from a DMAC having higher priority allowable even in a state such that DMA transfer processing is performed by some DMAC.

SOLUTION: When, for example, a bus request is made from a DMAC 2-1 having **higher priority** than another DMAC 2-2 has in a state such that the DMAC 202 makes **DMA transfer** processing with a shared memory 1, the DMAC 2-1 is made to acquire a bus by forcibly **interrupting the DMA transfer** processing after the time corresponding to a set **DMA transfer** cycle number has elapsed under the **DMA transfer interrupting**/terminating condition set on a register 6-1 correspondingly to the DMAC 2-2 or after the **transfer** processing ends.

DERWENT-ACC-NO: 1997-206172

DERWENT-WEEK: 199719

TITLE: **DMA** controlling method for data **transfer** between main memory and peripherals - has **interruption** controller which gives **priority** to new channel when **priority** of new channel is **higher** than current channel which is in operation

PATENT-ASSIGNEE: OKI ELECTRIC IND CO LTD[OKID]

PRIORITY-DATA: 1995JP-0052908 (March 13, 1995)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
JP 08249269 A	September 27, 1996	N/A	008	G06F 013/30

APPLICATION-DATA:

PUB-NO	APPL-DESCRIPTOR	APPL-NO	APPL-DATE
JP 08249269A	N/A	1995JP-0052908	March 13, 1995

INT-CL (IPC): G06F013/30

ABSTRACTED-PUB-NO: JP 08249269A

BASIC-ABSTRACT:

The method involves transferring data between memory and multiple input-output units based on a demand from the central processor. A channel retainer holds the number of channels by which the starting demand is carried out from the central processor. A priority channel number retainer (61) holds the priority of each channel, based on which input-output operation is carried out.

An execution channel number retainer (62) holds the number of channel indicated by the channel retainer and executes the data transfer operation. The channel retainer then holds the number of a new channel, while data transfer operation is performed through the previous channel. The execution of the transfer by the channel is interrupted temporarily, when the priority of new channel is higher. An interruption controller (70) gives priority to the interrupted channel and performs the transfer through that higher priority channel.

ADVANTAGE - Enables to perform transfer of channel with high priority preferably in burst transfer.

CHOSEN-DRAWING: Dwg.1/5

TITLE-TERMS: DMA CONTROL METHOD DATA TRANSFER MAIN MEMORY PERIPHERAL INTERRUPT CONTROL PRIORITY NEW CHANNEL PRIORITY NEW CHANNEL HIGH CURRENT CHANNEL OPERATE

DERWENT-CLASS: T01

EPI-CODES: T01-H03B; T01-H07A2;

SECONDARY-ACC-NO:
Non-CPI Secondary Accession Numbers: N1997-170117

US-PAT-NO: 5809335

DOCUMENT-IDENTIFIER: US 5809335 A

TITLE: Data transfer apparatus capable of handling DMA block transfer interruptions

DATE-ISSUED: September 15, 1998

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Kamiya; Yasuaki	Hamamatsu	N/A	N/A	JP

US-CL-CURRENT: 710/22, 710/23 , 710/264 , 710/28 , 710/40

ABSTRACT:

A method and a data transfer apparatus capable of handling DMA block transfer interruptions are provided. The data transfer apparatus includes a plurality of direct memory access (DMA) channels each having different priorities and at least one backup channel information memory for saving control information necessary for a restart of an interrupted DMA transfer through one of the DMA channels. The data transfer apparatus further includes a control means responsive to transfer commands which command DMA transfers through the DMA channels. In addition, the control means executes various interrupt handling steps when a transfer command interrupts an execution of a DMA transfer through one of the DMA channels having a lower priority than the priority of the DMA channel used by the interrupting transfer command, so that an interruption of an important data transfer can be prevented.

5 Claims, 12 Drawing figures

Exemplary Claim Number: 1

Number of Drawing Sheets: 11

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Detailed Description Text - DETX (17):

FIG. 5 shows an example of the relationship in timing between issuance of commands CHnGO for data transfer through **DMA** channels and states of the **DMA** channels and backup channels assumed when a **DMA** transfer through the **DMA** channel CH1 higher in priority than the **DMA** channel CH0 is commanded during **DMA** transfer through the **DMA** channel CH0. More specifically, when a command CH1GO for **DMA transfer** through the **DMA** channel CH1 **higher in priority** is issued during **DMA transfer** through the **DMA** channel CH0, channel information of the **DMA** channel CH0 lower in **priority** is saved into the backup channel BUPCH0 to **interrupt the DMA transfer** through the **DMA** channel CH0, whereby a **DMA transfer** through the **DMA** channel CH1 is preferentially carried out. When the **DMA** transfer through the **DMA** channel CH1 is completed, the information saved in the backup channel BUPCH0 is set to the **DMA** transfer-executing section 13, to thereby restart the interrupted **DMA** transfer through the backup channel BUPCH0.

Detailed Description Text - DETX (18):

FIG. 6 shows another example of the relationship in timing between issuance

of commands CHnGO for data transfer through DMA channels and states of the DMA channels and backup channels assumed when a DMA transfer through the DMA channel CH1 higher in priority than the DMA channel CH0 is commanded and then a DMA transfer through the DMA channel CH2 even higher in priority than the DMA channel CH1 is commanded during the DMA transfer through the DMA channel CH0. More specifically, when a command CH1GO for DMA transfer through the DMA channel CH1 is issued during DMA transfer through the DMA channel CH0 lower in priority than the DMA channel CH1, channel information of the channel CH0 is saved into the backup channel BUPCH0 to interrupt the DMA transfer through the DMA channel CH0, whereby a DMA transfer through the channel CH1 is preferentially carried out. However, when a command CH2GO for DMA transfer through the DMA channel CH2 even higher in priority is issued, channel information of the DMA channel CH1 lower in priority than the DMA channel CH2 is saved into the backup channel BUPCH1 to interrupt the DMA transfer through the DMA channel CH1. After completion of the DMA transfer through the DMA channel CH2, the later interrupted transfer, i.e., the DMA transfer through the DMA channel CH1 is restarted through the backup channel BUPCH1 higher in priority than the backup channel BUPCH0, and then, after completion of the DMA transfer through the backup channel BUPCH1, the first interrupted transfer, i.e., the DMA transfer through the DMA channel CH0, is restarted through the backup channel BUPCH0. Thus, all the transfers commanded are completed.

Detailed Description Text - DETX (20):

FIG. 8 shows a further example of the relationship in timing between issuance of commands CHnGO for data transfer through DMA channels and states of the DMA channels and backup channels assumed when DMA transfers through the DMA channels CH0 and CH1 are commanded during interruption of DMA transfers through the same DMA channels CH0 and CH1, which interruption has been caused by preferential execution of a DMA transfer through the DMA channel CH2 having the highest priority. More specifically, when a command CH1GO for DMA transfer through the DMA channel CH1 higher in priority than the DMA channel CH0 is issued during DMA transfer through the DMA channel CH0, channel information stored in the DMA channel CH0 is saved into the backup channel BUPCH0 to interrupt the transfer through the DMA channel CH0, whereby a DMA transfer through the DMA channel CH1 is preferentially carried out. Then, if a command CH2GO for DMA transfer through the DMA channel CH2 even higher in priority than the DMA channel CH1 is issued during the DMA transfer through the DMA channel CH1, channel information of the DMA channel CH1 lower in priority than the DMA channel CH2 is saved into the backup channel BUPCH1 as well, to interrupt the transfer through the DMA channel CH1, whereby a DMA transfer through the DMA channel CH2 is carried out. On this occasion, even if a new command CH1GO for DMA transfer through the DMA channel CH1 is issued, a transfer through the DMA channel CH1 lower in priority than the backup channel BUPCH1 is kept waiting. Therefore, after completion of the transfer through the DMA channel CH2, the transfer through the DMA channel CH1 is first restarted through the backup channel BUPCH1, and then the transfer through the channel CH1 which has been kept waiting is carried out. Similarly, when the transfer through the DMA channel CH1 is completed, the first interrupted transfer is restarted through the backup channel BUPCH0, and then a transfer through the DMA channel CH0 which has been kept waiting is carried out.

Detailed Description Text - DETX (21):

According to the present embodiment, as described above, the DMA channels CH0 to CH2 are set in the relationship of priority of CH2>CH1>CH0, and when a command for DMA transfer through a DMA channel CHn+1 higher in priority than a DMA channel CHn is issued during a DMA transfer through the DMA channel CHn, the DMA transfer through the DMA channel CHn is interrupted, whereby a DMA transfer through the DMA channel CHn+1 higher in priority is preferentially carried out. As a result, DMA transfer of data with a high degree of urgency

is promptly carried out without waiting.

Detailed Description Text - DETX (22):

Further, according to the present embodiment, a higher priority than that of a DMA channel CHn is imparted to a corresponding backup channel BUPCHn into which DMA channel information of the DMA channel CHn is saved, and when a DMA transfer through a DMA channel having a higher priority than that of the backup channel BUPCHn is completed, DMA transfers through the backup channel BUPCHn and the DMA channel CHn are successively restarted according to the priorities imparted thereto. As a result, even if a further command for DMA transfer through the DMA channel CHn which is kept waiting for DMA transfer is generated, restarting of the DMA transfer through the DMA channel CHn which has been interrupted by execution of a DMA transfer through a higher priority DMA channel is started with transfer of a data block which was about to be transferred at the last time of interruption of the DMA transfer through the DMA channel CHn, which makes it possible to achieve efficient and prompt interruption and restarting of the DMA block transfer.

Detailed Description Text - DETX (25):

As is shown in FIG. 10, when a DMA transfer through the DMA channel CH1 higher in priority than the DMA channel CH0 is commanded during a DMA transfer through the DMA channel CH0, channel information of the DMA channel CH0 is saved into the corresponding backup channel BUPCH0 to interrupt the DMA transfer through the DMA channel CH0, whereby the DMA transfer through the DMA channel CH1 higher in priority is carried out. During the DMA transfer through the DMA channel CH1, if a command for DMA transfer is issued for the DMA channel CH2 having an even higher priority, channel information of the channel CH1 cannot be saved into the backup channel BUPCH0 since the channel information of the DMA channel CH0 has already been saved into the backup channel BUPCH0, and therefore the transfer through the DMA channel CH1 is continued. Consequently, the DMA transfer through the DMA channel CH2 with the highest priority is suspended for a short time period until the transfer through the DMA channel CH1 is completed. Except for this, the DMA transfer according to the present embodiment is carried out in a manner identical with that carried out in the first embodiment described hereinbefore. In this embodiment, when a further command for DMA transfer through one channel is issued during a DMA transfer through the same channel, the new DMA transfer is kept waiting.

Claims Text - CLTX (11):

2. The data transfer apparatus of claim 1, wherein the control means is responsive to another transfer command issued while executing the interrupting transfer command such that the control means executes the another transfer command and interrupts the interrupting transfer command if the another transfer command uses one of the plurality of DMA channels having higher priority than the DMA channel used by the interrupting transfer command.